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09/607,815	06/30/2000	Kenneth W. Batcher	72255/02662	2193

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,815	BATCHER, KENNETH W.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buser et al., U.S. Patent Number 6,507,921 (herein referred to as Buser) in view of Zolnowsky et al., U.S. Patent Number 4,566,063 (herein referred to as Zolnowsky).

2. Referring to claim 1 Buser has taught a method of operating a processor to repeatedly execute a single instruction and to repeatedly execute a block of instructions (Buser column 22 lines 36-49).

Buser has not explicitly taught:

loading a register with a count value indicative of the number of times the associated instruction is to be executed;

fetching and executing a REPEAT instruction indicating the associated instruction to be repeatedly executed;

fetching the associated instruction; and

repeatedly executing the associated instruction for as many times as indicated by the count value.

Without refetching the associated instruction.

Zolnowsky hast taught:

loading a register with a count value indicative of the number of times the associated instruction is to be executed (Zolnowsky column 11 line 58-column 12 line 24; the register would have to be loaded with the count value);

fetching and executing a REPEAT instruction indicating the associated instruction to be repeatedly executed (Zolnowsky column 11 line 58-column 12 line 24);

fetching the associated instruction (Zolnowsky column 11 line 58-column 12 line 24); and

repeatedly executing the associated instruction for as many times as indicated by the count value (Zolnowsky column 11 line 58-column 12 line 24; any instruction in the loop is repeatedly executed, if there is one instruction in the loop, or up to 3 instructions).

Without refetching the associated instruction (Zolnowsky column 2 lines 9-12).

Buser has not explicitly taught the hardware or method that would be used to repeat the single instruction. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to look for details on how to perform a repeat instruction in a processor to be able to do a detailed design. Buser performs both single repeat operations and block repeat operations. Zolnowsky's system can be used to perform blocks of instructions, including a single instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to look to for details of the repeat operation system to be able to do a detailed design.

3. Referring to claim 8 Buser has taught a processor for repeatedly execute a single instruction and to repeatedly execute a block of instructions (Buser column 22 lines 36-49).

Buser has not explicitly taught:

load means for loading a register with a count value indicative of the number of times the associated instruction is to be executed;

first fetch means for a REPEAT instruction indicating the associated instruction to be repeatedly executed;

first execute means for executing the REPEAT instruction indicating the associated instruction to be repeatedly executed;

second fetch means for fetching the associated instruction; and

second execute means for repeatedly executing the associated instruction for as many times as indicated by the count value;

Without refetching the associated instruction.

Zolnowsky has taught:

load means for loading a register with a count value indicative of the number of times the associated instruction is to be executed (Zolnowsky column 11 line 58-column 12 line 24; the register would have to be loaded with the count value);

first fetch means for a REPEAT instruction indicating the associated instruction to be repeatedly executed (Zolnowsky column 11 line 58-column 12 line 24);

first execute means for executing the REPEAT instruction indicating the associated instruction to be repeatedly executed (Zolnowsky column 11 line 58-column 12 line 24);

second fetch means for fetching the associated instruction (Zolnowsky column 11 line 58-column 12 line 24; figure 8 shows two different paths for selecting the next instruction, or from the new PC); and

second execute means for repeatedly executing the associated instruction for as many times as indicated by the count value (Zolnowsky column 11 line 58-column 12 line 24; any instruction in the loop is repeatedly executed, if there is one instruction in the loop, or up to 3 instructions; figures 4-5, since the system uses multiple execution units, with each unit operating for most instructions, each execution part is considered a separate means);

Without refetching the associated instruction (Zolnowsky column 2 lines 9-12).

Buser has not explicitly taught the hardware or method that would be used to repeat the single instruction. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to look for details on how to perform a repeat instruction in a processor to be able to do a detailed design. Buser performs both single repeat operations and block repeat operations. Zolnowsky's system can be used to perform blocks of instructions, including a single instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to look to for details of the repeat operation system to be able to do a detailed design.

4. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buser in view of Shridhar et al, U.S. Patent Number 5,727,194 (herein referred to as Shridhar).

5. Referring to claim 2 Buser has taught a method of operating a processor to repeatedly execute a single instruction and to repeatedly execute a block of instructions (Buser column 22 lines 36-49).

Buser has not explicitly taught:

fetching a REPEAT instruction;

executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of tunes an associated instruction is to be executed;

fetching the associated instruction; and

repeatedly executing the associated instruction for as many times as indicated by the count value.

Shridhar has taught:

fetching a REPEAT instruction (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49);

executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of tunes an associated instruction is to be executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46);

fetching the associated instruction; and

repeatedly executing the associated instruction for as many times as indicated by the count value (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54).

Buser has not explicitly taught the hardware or method that would be used to repeat the single instruction. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to look for details on how to perform a repeat instruction in a processor to be able to do a detailed design. Buser performs both single repeat operations and block repeat operations. Shridhar's system can be used to perform blocks of instructions, including a single instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of

the invention to look to for details of the repeat operation system to be able to do a detailed design.

6. Referring to claim 3 Buser has taught a method of operating a processor to repeatedly execute a single instruction and to repeatedly execute a block of instructions (Buser column 22 lines 36-49).

Buser has not explicitly taught:

loading a register with a count value indicative of the number of times an associated instruction is to be executed;

fetching and executing a REPEAT instruction indicating the associated instruction that is to be repeatedly executed;

incrementing a program counter;

fetching the associated instruction; and

repeatedly executing the associated instruction for as many times as indicated by a count value stored in a count register.

Shridhar has taught:

loading a register with a count value indicative of the number of times an associated instruction is to be executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49);

fetching and executing a REPEAT instruction indicating the associated instruction that is to be repeatedly executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49);

incrementing a program counter (Shridhar column 15 lines 9-11 column 16 lines 15-20);

fetching the associated instruction (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49); and

repeatedly executing the associated instruction for as many times as indicated by a count value stored in a count register (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49).

Buser has not explicitly taught the hardware or method that would be used to repeat the single instruction. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to look for details on how to perform a repeat instruction in a processor to be able to do a detailed design. Buser performs both single repeat operations and block repeat operations. Shridhar's system can be used to perform blocks of instructions, including a single instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to look to for details of the repeat operation system to be able to do a detailed design.

7. Referring to claim 4 the combination of Buser and Shridhar has taught wherein said count value is stored in said count register before execution of said REPEAT instruction (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49; since the decode stage come before the fetch stage, as shown in figure 1, the information would be passed in the repeat circuitry before the repeat instruction was executed).

8. Referring to claim 5 the combination of Buser and Shridhar has taught wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register (Shridhar

figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49).

9. Referring to claim 6 the combination of Buser and Shridhar has taught wherein said method further comprises: incrementing the program counter after the associated instruction has been executed for as many times as indicated by the count value (Shridhar column 15 lines 9-11 column 16 lines 15-20 column 18 lines 13-15; the program would have to increment to the next address that it can continue executing the program outside of the loop).

10. Referring to claim 7 the combination of Buser and Shridhar has taught wherein method further comprises: decrementing said count value stored in said register each time said associated instruction is executed; and determining whether said count value is less than or equal to zero (Shridhar column 18 lines 31-38).

11. Claims 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buser in view of Kiuchi et al, U.S. Patent Number 5,579,493 (herein referred to as Kiuchi).

12. Referring to claim 9 Buser has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions (Buser column 22 lines 36-49).

Buser has not explicitly taught:

first fetch means for fetching a REPEAT instruction;

first execute means for executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times the instruction is to be executed;

second fetch means for fetching the associated instruction; and

second execute means for executing the associated instruction for as many times as indicated by the count value.

Kiuchi has taught:

first fetch means for fetching a REPEAT instruction (Kiuchi figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction);

first execute means for executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times the instruction is to be executed (Kiuchi figure 1 reference numbers 104,105; figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction);

second fetch means for fetching the associated instruction (Kiuchi figure 2 reference number 122,201; once repeating the instructions, the signal is sent out from 122,201 column 9 lines 18-26 figure 2 reference number 114,216 and 206; sends the signal to the selector in figure 1); and

second execute means for executing the associated instruction for as many times as indicated by the count value (Kiuchi figure 2; the execution means in figure 2 makes sure the associated instructions are executed for as many times as indicated in the count register).

Buser has not explicitly taught the hardware or method that would be used to repeat the single instruction. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to look for details on how to perform a repeat instruction in a processor to be able to do a detailed design. Buser performs both single repeat operations and block repeat operations. Kiuchi's system can be used to perform blocks of instructions, including a single instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of

the invention to look to for details of the repeat operation system to be able to do a detailed design.

13. Referring to claim 10 Buser has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions (Buser column 22 lines 36-49).

Buser has not explicitly taught:

load means for loading a register with a count value indicative of the number of times an instruction is to be executed;

first fetch means for fetching a REPEAT instruction indicating the associated instruction that is to be repeatedly executed;

first execute mean for executing the REPEAT instruction indicating the associated instruction that is to be repeatedly executed;

means for incrementing a program counter;

second fetch means for fetching the associated instruction; and

second execute means for repeatedly executing the associated instruction for as many times as indicated by a count value stored in a count register.

Kiuchi has taught:

load means for loading a register with a count value indicative of the number of times an instruction is to be executed (Kiuchi column 7 lines 18-31; there be required some loading means for the count to get into the correct register);

first fetch means for fetching a REPEAT instruction indicating the associated instruction that is to be repeatedly executed; (Kiuchi figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction);

first execute mean for executing the REPEAT instruction indicating the associated instruction that is to be repeatedly executed (Kiuchi figure 1 reference numbers 104,105; figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction);

means for incrementing a program counter (Kiuchi figure 1 reference numbers 104,105; figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction; the PC would have to be incremented, if not properly incremented, then the program would only fetch one instruction);

second fetch means for fetching the associated instruction (Kiuchi figure 2 reference number 122,201; once repeating the instructions, the signal is sent out from 122,201 column 9 lines 18-26 figure 2 reference number 114,216 and 206; sends the signal to the selector in figure 1); and

second execute means for repeatedly executing the associated instruction for as many times as indicated by a count value stored in a count register (Kiuchi figure 2; the execution means in figure 2 makes sure the associated instructions are executed for as many times as indicated in the count register).

Buser has not explicitly taught the hardware or method that would be used to repeat the single instruction. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to look for details on how to perform a repeat instruction in a processor to be able to do a detailed design. Buser performs both single repeat operations and block repeat operations. Kiuchi's system can be used to perform blocks of instructions, including a single instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of

the invention to look to for details of the repeat operation system to be able to do a detailed design.

14. Referring to claim 11 the combination of Buser and Kiuchi has taught wherein said count value is stored in said count register before execution of said REPEAT instruction (Kiuchi column 3 lines 38-56 column 2 lines 55-58; figure 1 reference numbers 104,105, since the information for the instruction is sent over the repeat control circuit from the decoder, the count will be stored before the repeat instruction is sent to the execution unit).

15. Referring to claim 12 the combination of Buser and Kiuchi has taught wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register (Kiuchi column 3 lines 38-56 column 2 lines 55-58).

16. Referring to claim 13 the combination of Buser and Kiuchi has taught wherein said processor further comprises: means for incrementing the program counter after the associated instruction has been executed for as many times as indicated by the count value (Kiuchi column 5 lines 37-42; the PC would have to be incremented after the repeat process was completed, otherwise it would not continue to execute other instructions in the program).

17. Referring to claim 14 the combination of Buser and Kiuchi has taught wherein processor further comprises:

means for decrementing said count value stored in said register each time said the instruction is executed; and

means for determining whether said count value is less than or equal to zero Kiuchi column 7 lines 33-44).

18. Referring to claim 15 Buser has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions (Buser column 22 lines 36-49).

Buser has not explicitly taught:

a memory address register associated with a main memory;

a memory data register associated with the main memory;

a memory control for generating memory control signals;

a program counter for storing a memory address location of the main memory where an instruction is to be fetched;

an instruction register for storing an instruction that is to be executed;

at least one general purpose register;

decode and execute control logic for decoding and executing an instruction stored in the instruction register; and

a state machine for controlling the fetching and repeated execution of an associated instruction.

Kiuchi has taught:

a memory address register associated with a main memory (Kiuchi column 8 lines 46-50);

a memory data register associated with the main memory (Kiuchi column 2 lines 30-36);

a memory control for generating memory control signals (Kiuchi column 3 lines 38-56);

a program counter for storing a memory address location of the main memory where an instruction is to be fetched (Kiuchi figure 1 reference number 106 column 5 lines 37-56);

an instruction register for storing an instruction that is to be executed (Kiuchi column 3 lines 9-22);

at least one general purpose register (Kiuchi column 12 lines 13-20; a register file);

decode and execute control logic for decoding and executing an instruction stored in the instruction register (Kiuchi figure 1 reference numbers 104,105 column 5 lines 37-56); and

a state machine for controlling the fetching and repeated execution of an associated instruction (Kiuchi column 6 lines 46-64; shows the different state the machine goes to implying a state machine).

Buser has not explicitly taught the hardware or method that would be used to repeat the single instruction. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to look for details on how to perform a repeat instruction in a processor to be able to do a detailed design. Buser performs both single repeat operations and block repeat operations. Kiuchi's system can be used to perform blocks of instructions, including a single instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to look to for details of the repeat operation system to be able to do a detailed design.

19. Referring to claim 16 the combination of Buser and Kiuchi has taught wherein said processor further comprises an instruction buffer for storing the associated instruction (Kiuchi figure 1 reference number 108).

21. Referring to claim 17 the combination of Buser and Kiuchi has taught wherein said general purpose register includes a first register for storing a count value indicative of the

number of times the one or more associated instructions are to be repeatedly executed (Kiuchi figure 2 reference number 207 column 7 lines 18-31).

21. Referring to claim 18 the combination of Buser and Kiuchi has taught wherein said state machine generates signals for decrementing the count value stored in the first register (Kiuchi column 7 lines 33-44).

22. Referring to claim 19 the combination of Buser and Kiuchi has taught wherein said state machine generates a signal for executing an instruction stored in said instruction register (Kiuchi column 1 lines 42-52; the states would have to have some indication of being ready to execute the instruction).

23. Referring to claim 20 the combination of Buser and Kiuchi has taught wherein said state machine generate a signal for incrementing said program counter after the associated instruction is repeatedly executed (Kiuchi column 7 lines 18-31; the program counter would be required to be incremented, otherwise only one instruction would ever be fetched for the entire system).

Referring to claim 21 the combination of Buser and Zolnowsky has taught wherein the means for executing the REPEAT instruction and the means for repeatedly executing the single instruction are the same means (Zolnowsky figure 1 reference number 12; the means for executing the repeat instruction and for repeatedly executing the single instruction are both in the processor of Zolnowsky).

Referring to claim 22 the combination of Buser and Zolnowsky Zolnowsky has taught wherein the means for fetching a REPEAT instruction and the means for fetching the single instruction are the same means (Zolnowsky figure 1 reference number 12; the means for fetching and for executing repeating are both in the processor of Zolnowsky).

Response to Arguments

Applicant's arguments with respect to claims filed on 04/13/04 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness
Examiner
Art Unit 2183
May 27, 2004

EDDIE CHAN
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